SPECIFICATION AMENDMENTS

Please replace paragraph 0018 with the following rewritten paragraph:

0018 The high-K gate dielectric 14B is preferably formed of metal oxides, metal silicates, metal nitrides, transition metal-oxides, transition metal silicates, metal aluminates, and transition metal nitrides, or combinations thereof. Preferably the dielectric constant of the gate dielectric layer 14B is greater than about 3.9. Exemplary preferred high-K gate dielectric materials include hafnium oxide (HfO_2), aluminum oxide (Al_2O_3), titanium oxide (TiO_2), tantalum oxide (Ta_2O_5)), zirconium oxide (ZrO_2), lanthanum oxide (La_2O_3), cerium oxide (CeO_2), bismuth silicate ($Bi_2Si_2O_{12}$), tungsten oxide (Wo3), yttrium oxide (Y_2O_3), lanthanum aluminate ($LaAlO_3$), barium strontium titanate ($Ba_xSr_xTiO_3$), strontium titanate ($SrTiO_3$), lead zirconate ($PbZrO_3$), PST, PZN, PZT, PMN, or combinations thereof. The gate dielectric material may be amorphous, polycrystalline~~silicon~~, crystalline, or combinations thereof.

Please replace paragraph 0020 with the following rewritten paragraph:

0020 It will be appreciated that the thickness of the high-K gat dielectric layer 14B will vary depending on the equivalent oxide thickness (EOT) desired, for example an[[d]] EOT of between about 5 Angstroms and 50 Angstroms. For example, the gate dielectric layer may vary between about 40 Angstroms and about 100 Angstroms.

Please replace paragraph 0021 with the following rewritten paragraph:

0021 Referring to Figure 1C, following formation of the high-K gate dielectric layer 14B, an overlying buffer layer 16 is formed over the high-K gate dielectric layer. The buffer layer 16 preferably has a dielectric constant of greater than about 3.9 and preferably has little or no[[t]] reactivity (bond forming reactions) with the high-K dielectric layer or the

subsequently formed overlying gate electrode. Preferably, the equivalent oxide thickness (EOT) for the buffer layer is less than the EOT of the high-K dielectric layer. The buffer layer is preferably doped with nitrogen, a metal or a semiconductor.

Please replace paragraph 0024 with the following rewritten paragraph:

0024 For example, exemplary buffer layer materials include aluminum oxide (e.g., Al_2O_3), aluminum silicate (e.g., $AlSi_xO_y$), or $AlSi_xO_yN_z$ for a PMOS gate structure and hafnium oxide (e.g., HfO_2), [[Hf]]hafnium silicate (e.g., $HfSi_xO_y$, or $HfSi_xO_yN_z$) for an NMOS device. It will be appreciated that the same buffer layer material may be included for both NMOS and PMOS devices, for example if a Si-metal bond formed at the buffer layer/gate electrode interface falls about midrange within an N or P doped polysilicon forbidden energy bandgap (E_g).

Please replace paragraph 0029 with the following rewritten paragraph:

0029 Following the gate etching process, plasma treatment processes with plasma source gases such as hydrogen, oxygen, nitrogen, ammonia, and mixtures thereof may be carried out including annealing treatments including one or more of the same preferred gases to form an annealing ambient. Referring to Figure 1F, conventional processes such as ion implantation to form source/drain doped regions (not shown) and form oxide and/or nitride offset liners e.g., 22A and/or offset spacers e.g., 22B are carried out to complete the formation of the MOSFET device.

Please replace paragraph 0030 with the following rewritten paragraph:

0030 Thus, a gate structure and method for forming the same has been presented to improve an electrical performance of a high-K gate dielectric. For example, the buffer layer formed on the top portion of the high-K gate dielectric according to preferred embodiments accomplishes several beneficial functions

including avoiding Fermi-level pinning at a high-K gate/gate electrode interface, for example caused by the formation of interface metal-Si bonds. The buffer layer is preferably doped with a dopant type and level to reduce a Voltage threshold (V_{th}) shift compared to the absence of the buffer layer. Preferably, the buffer dielectric layer dopant type and dopant level reduces Voltage threshold (V_{th}) shift to less than about half of the forbidden energy bandgap (Eg) at the gate electrode/doped buffer dielectric interface. For example, in an exemplary implementation, silicon (polysilicon) has a forbidden energy bandgap (E_g) of about 1.12 eV, where the buffer layer reduces the Voltage threshold shift to less than half that amount (e.g., $E_{g/2}$), even more preferably less than about one quarter of that amount.